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APPLICATION

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TITLE: GATE ESTIMATION PROCESS AND METHOD

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GATE ESTIMATION PROCESS AND METHOD

TECHNICAL FIELD

This invention relates to gate estimation during a semiconductor design process.

BACKGROUND

Integrated circuits typically incorporate various combinational elements (e.g., AND gates, OR gates, NAND gates, XOR gates, etc.) and state elements (e.g., latches, flip-flops, etc.) in their design. Each of these combinational and state elements are discrete elements that the engineer places into the circuit design.

The silicon wafers used in semiconductor chips have a finite surface area and each element (i.e., combinational and state) etched into these silicon wafers occupies a portion of that surface area. Accordingly, only a finite number of elements can be placed on one of these silicon wafers.

DESCRIPTION OF DRAWINGS

FIG. 1 is a diagrammatic view of the estimation process;

FIG. 2 is a diagrammatic view of the design space of the estimation process;

FIG. 3 is another diagrammatic view of the design space of the estimation process;

FIG. 4 is a diagrammatic view of the estimation method;

FIG. 5. is a diagrammatic view of another embodiment of the estimation process, including a processor and a computer readable medium; and

FIG. 6. is a diagrammatic view of another embodiment of the estimation process, including a processor and memory.

DETAILED DESCRIPTION

Referring to Figs. 1 and 2, there is shown a circuitry design system 10 that operates on a computer system 12 (e.g., a laptop computer, desktop computer, mainframe / thin client, etc.). A circuit designer 14 (e.g., a hardware engineer, a software engineer, etc.) utilizes circuitry design system 10 to design electronic circuits that may be incorporated into semiconductor devices, mounted on printed circuit boards, etc.

As circuitry design system 10 is a graphical system, designer 14 positions graphical representations of various circuitry components 16_{1-n} (e.g., AND gates, OR gates, NAND gates, XOR gates, latches, flip-flops, etc.) within a graphical representation of the circuit 18 being designed. During the design process, circuitry design system 10 provides contemporaneous feedback to designer 14 concerning one or more physical characteristics of the circuit 18 being designed.

Circuitry design system 10 includes an estimation process 20 for providing this feedback to designer 14. Estimation process 20 includes a parameter file maintenance process 22 for maintaining a circuit design parameter file 24 for the circuit 18 being designed by a circuit designer 14. This

circuit design parameter file 24 specifies at least one physical characteristic 26 of the circuit 18. Examples of these physical characteristics 26 include the total silicon area required to construct the circuit being designed; the total number of gates required to construct the circuit being designed; the total number of transistors required to construct the circuit being designed; the total number of cells required to construct the circuit being designed; the total amount of power required to power the circuit being designed; etc. This list is not intend to be all inclusive, as these physical characteristics 26 can be any other physical characteristic (e.g., intrinsic capacitance) associated with circuit 18. Files 24 are stored on some form of data repository 28 (e.g., a hard drive, a database, etc.)

Estimation process 20 includes a design space monitoring process 30 for monitoring circuitry design system 10 (i.e., a design environment) to detect the addition of a circuitry component 16_{1-n} to the circuit 18 being designed by designer 14.

When design space monitoring process 30 determines that a circuitry component 16_{1-n} has been added, a component file access process 32 accesses a component design parameter file 34 for that circuitry component. This component design parameter file 34 specifies at least one design parameter 38 for that particular type of circuitry component. These files 34 are also stored on data repository 30.

Each circuitry component 16_{1-n} added to circuit 18 is of a specific type (e.g., AND gate, OR gate, NAND gate, XOR gate, latch, d-flop, sr-flop, etc.). When a component 16_{1-n} is added to circuit 18, component file access process 32 first determines the type of circuitry component and then accesses a component design parameter file 34 for that particular type of circuitry component. For example, if designer 14 added a buffer 36 to circuit 18, design space monitoring process 30 would detect the addition of this buffer 36 to circuit 18. Component file access process 32 would then analyze this newly-added circuitry component 36 and determine that it is a buffer. Component file access process 32 would then retrieve the component design parameter file 34 for this particular type of circuitry component (i.e., a buffer). This file 34 would include at least one design parameter 38 specific for a buffer. Design parameter(s) 38 are related to the physical characteristic(s) 26 of circuit 18, as enumerated in circuit design parameter file 24. However, these design parameters 38 specify the physical characteristic as it relates to the discrete component 16_{1-n} being added and not the physical characteristic of the entire circuit 18. For example, if the physical characteristic 26 is the number of gates required to build the entire circuit, the design parameter 38 would be the number of gates required to build just the circuitry component being added.

Typically, higher-level circuitry components are produced by assembling lower-level circuitry components. For example,

three-input AND gate 40 is typically constructed from two two-input AND gates 42 and 44 placed in series. Additionally, a buffer (e.g., buffer 36) can be constructed from a two-input AND gate 46 with its input terminals tied together to form a single input. Accordingly, prior to installing buffer 36, circuit 18 has two buffers 48 and 50 and a three input AND gate 40. Therefore, the gate count of this circuit (in its current state) is four gates, namely one gate for each buffer 48 and 50 and two gates for the three-input AND gate 40.

Continuing with the above-stated example, when user 14 adds buffer 36 to circuit 18, the component design parameter file 34 for this buffer would indicate (via its design parameter 38) that this buffer 36 is constructed of a single gate. Therefore, the addition of buffer 36 to circuit 18 would add one additional gate to the total gate count for circuit 18. Accordingly, after buffer 36 is added to circuit 18, the physical characteristic 26 (i.e., the gate count) of circuit 18 (as specified in circuit design parameter file 24) would be changed from four to five.

Accordingly, a parameter file updating process 52 updates this circuit design parameter file 24 based on design parameter 38. Namely, since one buffer 36 is being added to circuit 18 and this buffer (pursuant to its design parameter 38) is constructed from one gate, the circuit design parameter file 24 will be updated to reflect the additional gate required to construct circuit 18. In this particular example,

this gate count represents the physical characteristic 26 specified in circuit design parameter file 24.

Allowing designer 14 to keep track of this physical characteristic (i.e., the gate count) allows the designer 14 to structure their design to meet (and not exceed) the physical capacities (e.g., size, maximum gate count, maximum transistor count, maximum cell count, maximum power draw, etc.) of the silicon wafer.

A feedback display process 54 provides designer 14 with feedback concerning the physical characteristic 26 being monitored by estimation process 20. This feedback can be automatically provided to designer 14, in that each time a circuitry component 16_{1-n} is added to circuit 18, feedback concerning this newly-updated physical characteristic 26 is displayed on the screen of computer 12. Alternatively, a feedback request process 56 may be incorporated into estimation process 20 so that feedback is only provided to designer 14 when they request the information. This request can be in the form of positioning the mouse pointer 58 over the newly-added device (i.e., buffer 36) so that a text box 60 appears which specifies the physical characteristic(s) 26 being monitored (in this example, the gate count). As an alternative, some other form of key strokes or mouse clicks can be indicative of a request by designer 14 to receive feedback concerning physical characteristic 26.

It is foreseeable that designer 14 may have to reconfigure circuit 18 during the design process and,

therefore, circuitry components 16_{1-n} may have to be deleted. Accordingly, design space monitoring process 30 is also configured to monitor circuitry design system 10 (i.e., the design environment) to detect the deletion of a circuitry component 16_{1-n} from the circuit 18 being designed. Further, component file access process 32 is configured to access a component design parameter file 24 that specifies at least one design parameter 26 for that deleted circuitry component. Additionally, parameter file updating process 52 is configured to update the circuit design parameter file 24 based on the design parameter(s) 38 included in the component design parameter file 34 for the deleted circuitry component.

As stated above, the physical characteristic 26 specified in circuit design parameter file 24 can be, among other things, the total silicon area required to construct the circuit being designed; the total number of gates required to construct the circuit being designed; the total number of transistors required to construct the circuit being designed; the total number of cells required to construct the circuit being designed; the total amount of power required to power the circuit being designed; etc.

Accordingly, estimation process 20 includes various processes 62, 64, 66, 98, and 100 for calculating and monitoring these various physical characteristics of circuit 18.

When the physical characteristic 26 is the total silicon wafer area required to construct the circuit being designed,

the related design parameter 38 specified in component design parameter file 34 would be the silicon area required to construct the added circuitry component.

In this case, parameter file updating process 52 includes an area recalculation process 62 for recalculating the total silicon area required to construct the circuit 18 being designed so that it includes the silicon area required to construct the added circuitry component.

Continuing with the above-stated example, when designer 14 adds buffer 36 to circuit 18, the design parameter 38 in component design parameter file 34 would specify the amount of silicon wafer surface area required to produce buffer 36. Accordingly, area recalculation process 62 sums the required surface area of circuit 18 prior to the addition of buffer 36 and the additional surface area required for buffer 36, to generate the new required surface area. Parameter file updating process 52 would then update circuit design parameter file 24 to reflect this new surface area.

When the physical characteristic 26 is the total number of gates required to construct the circuit being designed, the related design parameter 38 specified in component design parameter file 34 would be the number of gates required to construct the added circuitry component. In this case, parameter file updating process 52 includes a gate recalculation process 64 for recalculating the total number of gates required to construct the circuit 18 being designed so

that it includes the number of gates required to construct the added circuitry component.

Continuing with the above-stated example, when designer 14 adds buffer 36 to circuit 18, the design parameter 38 in component design parameter file 34 would specify that buffer 36 is constructed from one gate. Accordingly, gate recalculation process 64 sums the number of gates required to construct circuit 18 prior to the addition of buffer 36 (namely four) and the number of gates required to construct buffer 36 (namely one), to generate the new required number of gates (namely five). Parameter file updating process 52 would then update circuit design parameter file 24 to reflect this new gate count.

When the physical characteristic 26 is the total number of transistors required to construct the circuit being designed, the related design parameter 38 specified in component design parameter file 34 would be the number of transistors required to construct the added circuitry component

Transistors (of various types, MOSFETS, BJT, Heterostructures, etc.) are the building blocks of semiconductor circuits. In logic circuits, transistors act as switches to allow circuits to switch between binary states. Generally, AND gates, OR gates, NAND gates, XOR gates, latches, flip-flops, etc., are all constructed of transistors.

In this case (when the physical characteristic is a transistor count), parameter file updating process 52 includes

a transistor recalculation process 66 for recalculating the total number of transistors required to construct the circuit 18 being designed so that it includes the number of transistors required to construct the added circuitry component.

Referring to Figs. 1 and 3 and continuing with the above-stated example, circuit 68 in its current state has two, two-input NAND gates 70 and 72 connected to one, three-input NAND gate 74. The two, two-input NAND gates 70 and 72 can each be constructed from a pair of n-channel MOSFETs 76 and 78 and a pair of p-channel MOSFETs 80 and 82. Further, three-input NAND gate 74 can be constructed from three n-channel MOSFETs 84, 86, and 88 and three p-channel MOSFETs 90, 92, and 94. Accordingly, circuit 68 (in its current state) is constructed of fourteen transistors (four for each two-input NAND gate and six for the three-input NAND gate).

When designer 14 adds a third two-input NAND gate 96 to circuit 68, the design parameter 26 in component design parameter file 24 would specify that NAND gate 96 is constructed from four transistors. Accordingly, transistor recalculation process 66 sums the number of transistors required to construct circuit 68 prior to the addition of NAND gate 96 (namely fourteen) and the number of transistors required to construct NAND gate 96 (namely four), to generate the new required number of transistors (namely eighteen). Parameter file updating process 52 would then update circuit design parameter file 24 to reflect this new transistor count.

When the physical characteristic 26 is the total number of cells required to construct the circuit being designed, the related design parameter 38 specified in component design parameter file 34 would be the number of cells required to construct the added circuitry component

Cells are specific designated area on the surface of a silicon wafer, such that these areas can be etched (via photolithography) to produce a finite number of devices. These devices can be (on a macro level) circuitry components such as AND gates, OR gates, NAND gates, XOR gates, latches, flip-flops, etc. Alternatively, these devices can be (on a micro level), the transistors which are used to construct the circuitry components. Accordingly, a cell may be capable of having, for example, five transistors.

In this case (when the physical characteristic is a cell count), parameter file updating process 52 includes a cell recalculation process 98 for recalculating the total number of cells required to construct the circuit 68 being designed so that it includes the number of cells required to construct the added circuitry component.

As stated above, circuit 68 (prior to being modified) is constructed of fourteen transistors. If a maximum of five transistors can be incorporated into each transistor, circuit 68 (in its current state) would require three cells. When designer 14 adds a third two-input NAND gate 96 to circuit 68, the design parameter 38 in component design parameter file 34 would specify that NAND gate 96, which is constructed from

four transistors that would require one cell. Accordingly, cell recalculation process 98 sums the number of cells required to construct circuit 68 prior to the addition of NAND gate 96 (namely three) and the number of cells required to construct NAND gate 96 (namely one), to generate the new required number of cells (namely four). Parameter file updating process 52 would then update circuit design parameter file 24 to reflect this new cell count.

When the physical characteristic 26 is the total amount of power required to power the circuit being designed, the related design parameter 38 specified in component design parameter file 34 would be the amount of power required to power the added circuitry component

Each electronic device consumes electrical power during use. For illustrative purposes, let's assume that a transistor requires one milliwatt of power to function properly.

In this case (when the physical characteristic is power consumption), parameter file updating process 52 includes a power recalculation process 100 for recalculating the total amount of power required to power the circuit 68 being designed so that it includes the amount of power required to power the added circuitry component.

As stated above, circuit 68 (prior to being modified) is constructed of fourteen transistors. If each of these transistors has a maximum power consumption of 1 milliwatt, the original incarnation of this circuit consumes a maximum of

fourteen milliwatts. When designer 14 adds a third two-input NAND gate 96 to circuit 68, the design parameter 38 in component design parameter file 34 would specify that NAND gate 96, which is constructed from four transistors, would consume a maximum of four milliwatts. Accordingly, power recalculation process 100 sums the total amount of power required to power circuit 68 prior to the addition of NAND gate 96 (namely fourteen milliwatts) and the amount of power required to power NAND gate 96 (namely four milliwatts), to generate the new required amount of power namely eighteen milliwatts). Parameter file updating process 52 would then update circuit design parameter file 24 to reflect this new power requirement.

As stated above, the physical characteristic 26 specified in circuit design parameter file 24 can be, among other things, the total silicon area required to construct the circuit being designed; the total number of gates required to construct the circuit being designed; the total number of transistors required to construct the circuit being designed; the total number of cells required to construct the circuit being designed; the total amount of power required to power the circuit being designed; etc. While thus far, estimation process 20 has been shown to provide feedback to designer 14 concerning only one of these physical characteristics 26, this is for illustrative purposes only and is not intended to be a limitation of the invention. Specifically, estimation process 20 can provide feedback to designer 14 concerning as many (or

as few) physical characteristics 26 as needed, required, or desired.

Referring to Fig. 4, there is shown an estimation method 110 that maintains 112 a circuit design parameter file for a circuit being designed by a circuit designer. The circuit design parameter file specifies a physical characteristic of the circuit. Method 110 monitors 114 a design environment to detect the addition of a circuitry component to the circuit. Method 110 accesses 116 a component design parameter file that specifies at least one design parameter for that added circuitry component and updates 118 the circuit design parameter file based on the at least one design parameter included in the component design parameter file.

Method 110 provides 120 the circuit designer with feedback concerning the physical characteristic of the circuit being designed. Method 110 allows 122 the circuit designer to request feedback concerning the physical characteristic of the circuit being designed and provides 124 the circuit designer with feedback concerning the physical characteristic of the circuit being designed in response to the circuit designer requesting the same.

The physical characteristic is the total silicon area required to construct the circuit being designed and the at least one design parameter is the silicon area required to construct the added circuitry component. Updating 118 the circuit design parameter file includes recalculating 126 the total silicon area required to construct the circuit being

designed so that it includes the silicon area required to construct the added circuitry component.

The physical characteristic is the total number of gates required to construct the circuit being designed and the at least one design parameter is the number of gates required to construct the added circuitry component. Updating 118 the circuit design parameter file includes recalculating 128 the total number of gates required to construct the circuit being designed so that it includes the number of gates required to construct the added circuitry component.

The physical characteristic is the total number of transistors required to construct the circuit being designed and the at least one design parameter is the number of transistors required to construct the added circuitry component. Updating 118 the circuit design parameter file includes recalculating 130 the total number of transistors required to construct the circuit being designed so that it includes the number of transistors required to construct the added circuitry component.

The physical characteristic is the total number of cells required to construct the circuit being designed and the at least one design parameter is the number of cells required to construct the added circuitry component. Updating 118 the circuit design parameter file includes recalculating 132 the total number of cells required to construct the circuit being designed so that it includes the number of cells required to construct the added circuitry component.

The physical characteristic is the total amount of power required to power the circuit being designed and the at least one design parameter is the amount of power required to power the added circuitry component. Updating 118 the circuit design parameter file includes recalculating 134 the total amount of power required to power the circuit being designed so that it includes the amount of power required to power the added circuitry component.

Method 110 further includes monitoring 136 a design environment to detect the deletion of a circuitry component from the circuit being designed. Method 110 further includes accessing 138 a component design parameter file that specifies at least one design parameter for that deleted circuitry component. Method 110 further includes updating 140 the circuit design parameter file based on the at least one design parameter included in the component design parameter file for that deleted circuitry component.

Referring to Fig. 5, there is shown a computer program product 250 residing on a computer readable medium 252 having a plurality of instructions 254 stored thereon. When executed by processor 256, instructions 254 cause processor 256 to maintains 258 a circuit design parameter file for a circuit being designed by a circuit designer. The circuit design parameter file specifies a physical characteristic of the circuit. Computer program product 250 monitors 260 a design environment to detect the addition of a circuitry component to the circuit. Computer program product 250 accesses 262 a

component design parameter file that specifies at least one design parameter for that added circuitry component and updates 264 the circuit design parameter file based on the at least one design parameter included in the component design parameter file.

Typical embodiments of computer readable medium 252 are: hard drive 266; tape drive 268; optical drive 270; RAID array 272; random access memory 274; and read only memory 276.

Now referring to Fig. 6, there is shown a processor 300 and memory 302 configured to maintain 304 a circuit design parameter file for a circuit being designed by a circuit designer. The circuit design parameter file specifies a physical characteristic of the circuit. Processor 300 and memory 302 monitor 306 a design environment to detect the addition of a circuitry component to the circuit. Processor 300 and memory 302 access 308 a component design parameter file that specifies at least one design parameter for that added circuitry component and update 310 the circuit design parameter file based on the at least one design parameter included in the component design parameter file.

Processor 300 and memory 302 may be incorporated into a personal computer 312, a network server 314, or a single board computer 316.

Other embodiments are within the scope of the following claims.